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[PFET-BASED ESD PROTECTION STRATEGY FOR IMPROVED EXTERNAL LATCH-UP ROBUSTNESS]

Abstract

A method and apparatus for protection against electrostatic discharge (ESD) with improved latch-up robustness featuring a silicide blocked p-type field effect transistor is disclosed. The transistor has a snapback voltage that is less than the breakdown voltage of its gate oxide. The transistor is part of an integrated circuit and coupled to an I/O pad having no n-diffusions connected directly to it. A given integrated circuit may employ one or more the transistors configured in accordance with the invention that are associated with one or more I/O pads within the integrated circuit.